CLAIMS

1. A semiconductor construction comprising:

a pair of gate structures supported by a semiconductive material; and

an isolation region between the pair of gate structures, the isolation region comprising:

an indium doped pocket within the semiconductive material, the pocket region comprising a first width; and

a third gate structure over the pocket region, the third gate structure comprising a gate stack having a lateral width that is greater than the first width.

2. The semiconductor structure of claim 1 wherein the pocket region comprises an indium concentration from about 1×10^{12} atoms/cm^3 to about 1×10^{13} atoms/cm^3.

3. The semiconductor construction of claim 1 further comprising a pair of source/drain regions that extend partially under the third gate structure, the source/drain regions being majority doped with an n-type dopant and wherein the gate stack of third gate structure comprises a layer of conductively doped material majority doped with a p-type dopant.

4. The semiconductor construction of claim 3 wherein the conductively doped material comprises at least 1 x 10^{18} atoms/cm^3 n-type dopant and at least 1 x 10^{18} atoms/cm^3 p-type dopant.

5. The semiconductor construction of claim 1 wherein the pair of gate structures comprise a pair of transistors having transistor stacks, each of the transistor stacks having a transistor stack width, wherein each of the transistors is disposed over a channel region defined within the semiconductive material, each channel region comprising an indium doped channel pocket having a pocket width that is less than the transistor stack width.

6. The semiconductor construction of claim 5 wherein the channel regions are additionally doped with from about 1 x 10^{12} atoms/cm^3 to about 2 x 10^{12} atoms/cm^3 boron.

7. The semiconductor construction of claim 1 wherein each of the pair of gate structures comprises:

a layer of polysilicon ; and

a metal material over the layer of polysilicon, the metal material having a planarized upper surface.

8. A semiconductor construction comprising:

a pair of gate structures supported by a semiconductive material; and

an isolation region between the pair of gate structures, the isolation region comprising an indium doped pocket within the semiconductive material.

9. The semiconductor construction of claim 8 wherein each of the pair of gate structures comprises a layer comprising tungsten.

10. A semiconductor construction comprising:

a pair of channel regions a within a semiconductive material, at least a portion of each of the channel regions being an indium doped sub-region, each indium doped sub-region having a first width; and

a pair of transistor constructions separated by an isolation region which isolates the transistor constructions from one another, each transistor construction being disposed over a channel region comprised by the pair of channel regions, each of the transistor constructions comprising a transistor gate having a second width that is greater than the first width, each of the gates being substantially laterally centered over the corresponding channel region.

11. The semiconductor structure of claim 10 wherein the isolation region comprises a shallow trench isolation region.

12. The semiconductor structure of claim 10 wherein the isolation region comprises an isolation gate having a first conductively-doped material separated from a second conductively-doped material by an intervening insulative material; the first conductively doped material comprises a p-type majority dopant, and further comprising a lack of indium doped pocket beneath the isolation gate.

13. The semiconductor structure of claim 10 wherein the isolation region comprises an isolation gate, and further comprising a doped pocket region disposed in the substrate underlying the isolation gate and being substantially laterally centered relative to the isolation gate.

14. The semiconductor substrate of claim 13 wherein the doped pocket region is lightly doped with indium and wherein the isolation gate comprises a first conductively-doped material separated from a second conductively-doped material by an intervening insulative material; and wherein a majority dopant in the first conductively doped material is p-type.

15. The semiconductor substrate of claim 13 wherein at least part of the doped pocket region is indium doped.

16. A semiconductor construction comprising:

a field effect transistor having an access side and an opposing bitline side;

a pair of source/drain regions associated with the field effect transistor; one of the source/drain regions being on the access side and the other source/drain region being on the bitline side of the field effect transistor device; and

an indium implant associated with only one of the pair of source/drain regions.

17. The semiconductor construction of claim 16 wherein the indium implant is associated with the source/drain region on the bitline side of the field effect transistor.

18. A semiconductor construction comprising:

a semiconductor substrate

a pair of conductively doped diffusion regions within a semiconductive material of the substrate, the conductively doped diffusion regions comprising a first type of dopant;

a transistor construction over the substrate, the transistor construction comprising:

a gate disposed between the pair of diffusion regions and having a pair of opposing sidewalls;

spacers disposed along the opposing sidewalls, the conductively doped diffusion regions extending under the spacers; and

a diffusion region extension present on a first side of the transistor construction and absent on an opposing second side of the transistor construction, the diffusion region extension comprising a second type of dopant and extending the diffusion region farther beneath the transistor construction on the first side of the transistor construction relative to the diffusion region on the second side of the transistor construction.

19. The semiconductor construction of claim 18 wherein the first type of dopant is an n-type and the second type dopant is a p-type.

20. The semiconductor construction of claim 18 wherein the second type dopant is indium.

21. The semiconductor construction of claim 18 wherein the diffusion region comprising the diffusion region extension is associated with a bitline contact.

22. A semiconductor construction comprising:

a semiconductive material substrate;

a first and a second transistor construction over the semiconductive substrate material, each of the first and second transistor constructions having opposing sidewalls with a pair of insulative spacers along the sidewalls;

a first and a second source/drain region within the substrate, the first transistor construction being disposed between the first and the second source/drain regions, a first end of the first source/drain region extending beneath the spacer on a first side of the first transistor construction and the second source/drain region extending beneath the spacer on an opposing second side of the first transistor construction;

a third and a fourth source/drain region within the substrate, the second transistor construction being disposed between the third and fourth source/drain regions, a first side of the fourth source/drain region extending beneath the spacer on a first side of the second transistor construction, and the third source/drain region extending beneath the spacer on an opposing second side of the second transistor construction; the first, second, third and fourth source/drain regions being commonly doped with a first type of dopant;

a source/drain extension associated with the first side of the first source/drain region, the source/drain extension being doped with a second type of dopant and extending the first side of the first source/drain region farther beneath the first transistor construction; extensions being absent from a second side of the first source/drain region, and absent from the second source/drain region.

23. The semiconductor construction of claim 22 further comprising channel regions defined within the substrate beneath each of the first and second transistor constructions at least a portion of the channel regions being doped with indium.

24. The semiconductor construction of claim 22 further comprising a source/drain extension associated with the first side of the fourth source/drain region, the source/drain extension being doped with a second type of dopant and extending the first side of the fourth source/drain region farther beneath the second transistor construction; extensions being absent from a second side of the fourth source/drain region, and absent from the third source/drain region.

25. The semiconductor construction of claim 22 further comprising an isolation structure between the first and second transistor constructions.

26. The semiconductor construction of claim 25 further comprising a doped pocket region within the semiconductive material beneath the isolation structure, at least a portion of the pocket region being doped with indium.

27. The semiconductor construction of claim 25 wherein the isolation structure comprises a first conductively-doped material separated from a second conductively-doped material by an intervening insulative material; the first conductively-doped material being doped to at least 1 x 10^{18} atoms/cm^3 with n-type dopant and to at least 1 x 10^{18} atoms/cm^3 with p-type dopant.

28. The semiconductor construction of claim 27 wherein a majority dopant in the first conductively doped material is p-type.

29. The semiconductor construction of claim 28 having an absence of any indium implant beneath the isolation structure.

30. The semiconductor construction of claim 28 having a lightly doped indium implant beneath the isolation structure.

31. The semiconductor construction of claim 22 further comprising a shallow trench isolation region between the first and the second transistor constructions.

32. A DRAM construction comprising:

a first and a second gate structure;

four nodes, the four nodes comprising a first node, a second node, a third node and a fourth node, the first node being in gated electrical connection with the second node through the first gate structure, and the third node location being in gated electrical connection with the fourth node location through the second gate structure; each of the four nodes having a diffusion region associated therewith, the diffusion regions associated with the first and second nodes each extending under the first gate structure, and the diffusion regions associated with the third and fourth nodes extending under the second gate structure;

an isolation region between the second and third nodes, the isolation region electrically isolating the first and the second gate structures from one another;

a bit line contact in electrical connection with the first node;

a capacitor construction in electrical connection with the second node, the capacitor construction comprising a storage node;

an indium implant in the diffusion region associated with the first node, the implant being under the first gate structure proximate the first node; and

an absence of an indium implant in the diffusion region associated with the second node.

33. The DRAM construction of claim 32 wherein the indium implant is a first indium implant and further comprising:

a second indium implant, the second indium implant being in the diffusion region associated with the fourth node and under the second gate, wherein the fourth node is in electrical connection with a bitline contact; and

an absence of an indium implant associated with the diffusion region associated with the third node.

34. The DRAM construction of claim 32 wherein the isolation region comprises an isolation structure having a total width, and further comprising a doped pocket beneath the isolation structure, the doped pocket comprising a width that is less than or equal to about half a total width of the isolation structure.

35. The DRAM construction of claim 32 wherein each of the gate structures comprises opposing gate sidewalls and a pair of insulative spacers having inside surfaces along and against the gate sidewalls and having outside surfaces away from the sidewalls, each gate structure comprising a total width corresponding to the greatest distance between the outside surfaces of the pair of insulative spacers associated with the corresponding gate; and wherein the DRAM construction further comprises conductively doped channel regions beneath each of the gate structures, at least a portion of the channel regions being doped with indium, the portion comprising a width that is less than or equal to about half the total width of the gate structure.

36. A method of forming a doped region in a semiconductor substrate comprising:

forming a pair of blocks over a semiconductive material of a semiconductor substrate, the pair of blocks being spaced from each other by a gap comprising a first distance;

narrowing the gap; and

implanting dopant into the semiconductive material though the narrowed gap to form a doped region in the semiconductive material.

37. The method of claim 36 wherein the blocks comprise patterned photoresist and having opposing sidewalls, and wherein the narrowing the gap comprises:

forming a coating over the patterned photoresist and over the substrate within the gap; and

selectively removing the coating from over at least a portion of the substrate within the gap while leaving the coating on the photoresist block, the coating material forming sidewall extensions against the opposing sidewalls.

38. The method of claim 36 wherein the implanting dopant through the narrowed gap comprises implanting indium to a concentration of from about 1×10^{12} atoms/cm^3 to about 1×10^{13} atoms/cm^3.

39. The method of claim 36 wherein the implanting dopant through the narrowed gap comprises implanting boron to a concentration of from about 1×10^{12} atoms/cm^3 to about 2×10^{12} atoms/cm^3, and implanting indium to a concentration of from about 1×10^{12} atoms/cm^3 to about 1×10^{13} atoms/cm^3.

40. The method of claim 36 wherein the implanting dopant through the narrowed gap comprises implanting a second dopant, the method further comprising implanting a first dopant into the semiconductive material prior to implanting the second dopant.

41. The method of claim 40 wherein the first dopant comprises boron and the second dopant comprises indium.

42. The method of claim 40 wherein the implanting the first dopant occurs prior to extending the blocks.

43. The method of claim 40 wherein the implanting the first dopant occurs during the narrowing the gap.

44. The method of claim 36 further comprising activating the dopant at a temperature of about 900°C for between about 1 minute to about 6 minutes.

45. A method of forming a semiconductor construction, comprising:

forming a layer of patternable material over a semiconductive substrate material;

patterning the layer of patternable material to form at least two patterned blocks, a pair of adjacent blocks being separated by a first gap;

forming a coating over the pair of adjacent blocks and across the first gap between the adjacent blocks;

selectively removing the coating from across the first gap while leaving the coating on the pair of adjacent blocks; the pair of blocks and coating together defining a pair of enlarged blocks that are separated by a second gap; the second gap being narrower than the first gap;

while the enlarged blocks remain over the semiconductive substrate material, implanting at least one dopant within the semiconductive material within the second gap to form a doped region; and

removing the enlarged blocks from over the semiconductive substrate material.

46. The method of claim 45 wherein the patternable material comprises photoresist and wherein the coating comprises a material which cross-links when exposed to the acid from the photoresist.

47. The method of claim 45 wherein the coating corresponds to a material designated as AZ R200™ by Clariant International, Ltd.

48. The method of claim 45 wherein the patterned blocks are formed by a photolithographic process; wherein the photolithographic process is limited to a minimum feature size that can be obtained by the photolithographic process, the first gap corresponding to about the minimum feature size; and wherein the doped region of the semiconductive material formed by the implanting has a region width that is less than the minimum feature size.

49. The method of claim 48 wherein the region width is less than or equal to about 50% of the minimum feature size.

50. The method of claim 45 further comprising:

forming a first source/drain region and a second source/drain region within the semiconductive substrate material, the first source/drain region being laterally spaced from a first edge of the doped region and the second source/drain region being laterally spaced from a second opposing edge of the doped region; and

forming an isolation mass over the doped region, the first and second source/drain regions extending partially under the isolation mass.

51. The method of claim 50 wherein the isolation mass comprises a gate stack, the gate stack comprising a layer of conductively doped material separated from the doped region by an insulative material layer, the layer of conductively doped material being majority doped with a p-type dopant, and wherein the source/drain regions are majority doped with an n-type dopant.

52. The method of claim 50 further comprising forming a pair of transistor devices over the semiconductor substrate, the transistor devices being electrically isolated from one another by the isolation mass.

53. A DRAM forming method comprising:

forming a first wordline and a second wordline over a substrate, each wordline comprising a pair of opposing sidewalls;

defining four nodes proximate the wordlines, the four nodes comprising a first node, second node, third node and fourth node, the second node being in gated electrical connection with the first node through the first wordline, and the fourth node being in gated electrical connection with the third node through the second wordline;

defining a first, second, third and fourth diffusion regions, the first diffusion region being associated with the first node, the second diffusion region being associated with the second node, the third diffusion region being associated with the third node, and the fourth diffusion region being associated with the fourth node;

defining an isolation region between the first wordline and the second wordline, the isolation region electrically isolating the first and second wordlines from each other;

forming a pair of spacers along opposing sidewalls of each wordline; the first and second diffusion regions extending an initial distance under the first wordline, and the third and fourth diffusion regions extending an initial distance under the second wordline; and

extending the first diffusion region farther under the first wordline relative to the initial distance without extending the second diffusion region.

54. The method of claim 53 further comprising extending the fourth diffusion region farther under the second wordline relative to the initial distance without extending the third diffusion region.

55. The method of claim 53 wherein the spacers comprise a spacer width and wherein the initial distance is less than the spacer width.

56. The method of claim 53 wherein each of the diffusion regions are conductively doped with a first type dopant and wherein the extending comprises halo implanting a second type dopant.

57. The method of claim 53 wherein the diffusion regions are majority doped with n-type dopant and wherein the extending comprises forming extension regions majority doped with p-type dopant.

58. The method of claim 53 wherein the isolation region comprises a shallow trench isolation region.

59. The method of claim 53 further comprising:

forming a first and second capacitor constructions; the first capacitor construction being in electrical connection with the second node, and the second capacitor construction being in electrical connection with the third node; and

forming a first bit line contact in electrical connection with the first node and a second bit line contact in electrical connection with the third node.

60. The method of claim 53 wherein the defining an isolation region comprises:

forming a doped pocket region within the semiconductor substrate, the doped pocket region comprising a pocket width; and

forming an isolation mass over the substrate and over the pocket region, the isolation mass having a total mass width that is greater than the pocket width.

61. The method of claim 60 wherein the isolation mass comprises:

a gate stack over the substrate, the gate stack having opposing sidewalls;

a pair of insulative spacers along the opposing sidewalls, the total mass width being a distance between outer edges of the pair of insulative spacers measured at a surface of the substrate; and

wherein the total mass width is at least about double the pocket width.

62. A method of forming a semiconductor construction, comprising:

forming a dielectric material over a semiconductive substrate material;

patterning the dielectric material to form at least two patterned blocks, a pair of adjacent blocks being separated by a first gap, each block having a sidewall within the first gap;

forming a pair of spacers along the sidewalls and within the first gap, the spacers having lateral edges separated by a gap, the second gap being narrower than the first gap;

while the spacers remain along the sidewalls, implanting at least one dopant into the semiconductive material within the second gap to form a doped region; and

removing the spacers from along the sidewalls.

63. The method of claim 62 further comprising after removing the spacers, forming a layer of polysilicon over the semiconductive material within the gap and along the sidewalls.

64. The method of claim 63 further comprising:

depositing a material comprising at least one of a metal and a metal nitride over the polysilicon layer; and

planarizing the material.